CLAIMS

What is claimed is:

1. A system comprising:

a processor; and

a memory device coupled to the processor and comprising:

a regulator control coupled to an external voltage source; and

a plurality of internal voltage buses coupled to the regulator control to provide power to a plurality of circuits, wherein at least one of the plurality of internal voltage buses comprises a plurality of control circuitry having at least one level shifter configured to:

receive at least one disable signal and at least one data signal;

provide a determined output signal when the at least one disable signal corresponds to a deep power down mode; and

provide an output signal that is based on the at least one data signal when the at least one disable signal does not correspond to the deep power down mode.

2. The system, as set forth in claim 1, wherein the plurality of internal voltage buses comprises an operating voltage bus that provides an operating voltage to output buffer circuitry.

3. The system, as set forth in claim 1, wherein the plurality of internal voltage buses comprises an array voltage bus that provides an array voltage to array circuitry.

4. The system, as set forth in claim 1, wherein the processor is coupled to a communication port.

5. The system, as set forth in claim 1, wherein the processor is coupled to an input device.

6. The system, as set forth in claim 1, wherein the processor is coupled to a display.

7. The system, as set forth in claim 1, wherein the control circuitry comprises at least one of an operating voltage control circuitry and a delay lock loop control circuitry.

8. The system, as set forth in claim 7, wherein the at least one level shifter in the at least one of an operating voltage control circuitry and a delay lock loop control circuitry comprises:

a first transistor coupled between a first output terminal and a low voltage source; and

a second transistor coupled between a second output terminal and the low voltage source, wherein the first and second transistors are configured to:

receive the at least one disable signal;

couple the first output terminal and the second output terminal to the low voltage source if the at least one disable signal corresponds to the deep power down mode; and

isolate the first output terminal and the second output terminal from the low voltage source if the at least one disable signal does not correspond to the deep power down mode.

9. The system, as set forth in claim 8, wherein the at least one level shifter in the at least one of an operating voltage control circuitry and the delay lock loop control circuitry comprises a third transistor coupled between the external voltage source and level shifter circuitry, wherein the third transistor is configured to:

receive the at least one disable signal;

isolate the level shifter circuitry from the external voltage source if the at least one disable signal does not correspond to the deep power down mode; and

couple the level shifter circuitry to the external voltage source if the at least one disable signal corresponds to the deep power down mode.

10. The system, as set forth in claim 1, wherein the regulator control comprises a plurality of grounding devices coupled between one of the plurality of internal voltage buses and a low voltage source, wherein each of the plurality of grounding devices is configured to:

receive the at least one disable signal;

isolate the one of the plurality of internal voltage buses from the low voltage source if the at least one disable signal does not correspond to the deep power down mode; and

couple the one of the plurality of internal voltage buses to the low voltage source if the at least one disable signal corresponds to the deep power down mode.

11. The system, as set forth in claim 10, wherein the one of the plurality of grounding devices comprises:

a transistor having a drain, a source, and a gate;

wherein the drain of the transistor is coupled between a resistor coupled to the one of the plurality of internal voltage buses and a voltage logic coupled to an external voltage source;

the source of the transistor coupled to the low voltage source; and

the gate of the transistor coupled to an input configured to receive the at least one disable signal.

12. A system comprising:

a processor; and

a memory device coupled to the processor and comprising:

a regulator control coupled to an external voltage source;

an internal voltage bus coupled to the regulator control to receive power from the regulator control; and

an output buffer circuitry coupled to the internal voltage bus and having at least one level shifter, the output buffer circuitry configured to:

receive at least one disable signal and at least one data signal;

provide a predetermined output signal if the at least one disable signal corresponds to a deep power down mode, regardless of the at least one data signal; and

provide an output signal that is based on the at least one data signal if the at least one disable signal does not correspond to the deep power down mode.

13. The system, as set forth in claim 12, wherein the at least one data signal comprises a first disable signal and a second disable signal.

14. The system, as set forth in claim 13, wherein the at least one level shifter in the output buffer circuitry comprises:

a first transistor coupled between an output terminal and an output pad voltage source, the first transistor configured to:

receive the first disable signal;

couple the output terminal to the output pad voltage source if the first disable signal corresponds to the deep power down mode; and

isolate the output terminal to the output pad voltage source if the first disable signal does not correspond to the deep power down mode.

15. The system, as set forth in claim 14, wherein the at least one level shifter in the output buffer circuitry comprises:

a second transistor coupled between the output terminal and a low output pad voltage source, and

a third transistor coupled between a gate of the second transistor and a low voltage source,

wherein the third transistor is configured to:

receive the second disable signal;

prevent the second transistor from coupling the output terminal to the low output pad voltage source if the second disable signal corresponds to the deep power down mode; and

permit the second transistor to couple the output terminal to the output pad voltage source if the second disable signal does not correspond to the deep power down mode.

16. The system, as set forth in claim 12, wherein the at least one data signal comprises a first disable signal, a second disable signal, and a third disable signal.

17. The system, as set forth in claim 16, wherein the at least one level shifter in the output buffer circuitry comprises:

a first transistor coupled between an output terminal and a low output pad voltage source, wherein the first transistor is configured to:

receive the first disable signal;

couple the output terminal to the low output pad voltage source if the first disable signal corresponds to the deep power down mode; and

isolate the output terminal from the low output pad voltage source if the first disable signal does not correspond to the deep power down mode.

18. The system, as set forth in claim 17, wherein the at least one level shifter in the output buffer circuitry comprises:

a second transistor coupled between a gate of a third transistor and an output pad voltage source, wherein the second transistor is configured to:

receive the second disable signal;

prevent the gate of the third transistor from closing if the second disable signal corresponds to the deep power down mode; and

permit the gate of the third transistor to close if the second disable signal does not correspond to the deep power down mode.

19. The system, as set forth in claim 18, wherein the at least one level shifter in the output buffer circuitry comprises:

a fourth transistor coupled between a gate of a fifth transistor and the low output pad voltage source, wherein the fourth transistor is configured to:

receive the third disable signal;

prevent the gate of the fifth transistor from closing if the third disable signal corresponds to the deep power down mode; and

permit the gate of the fifth transistor to close if the third disable signal does not correspond to the deep power down mode.

20. A memory device comprising:

a regulator control coupled to an external voltage source;

a voltage bus coupled to the regulator control to provide power to a plurality of circuits,

a control circuitry coupled to the voltage bus having a level shifter that is configured to:

receive a disable control signal and a data signal;

provide a predetermined output signal when the disable control signal corresponds to a deep power down mode;

provide an output signal that is based on the data signal when the disable control signal does not correspond to a deep power down mode.

21. The memory device, as set forth in claim 20, wherein the memory device comprises a dynamic random access memory (DRAM) device.

22. The memory device, as set forth in claim 20, wherein the memory device comprises a static random access memory (SRAM) device.

23. The memory device, as set forth in claim 20, wherein the regulator control comprises a grounding device configured to ground the voltage bus when a deep power down signal is received at the regulator control.

24. The memory device, as set forth in claim 20, wherein the plurality of circuits comprises output buffer circuitry.

25. The memory device, as set forth in claim 20, wherein the plurality of circuits comprises delay lock loop circuitry.

26. The memory device, as set forth in claim 20, wherein the level shifter comprises:

a first transistor coupled between a first output terminal and a low voltage source; and

a second transistor coupled between a second output terminal and the low voltage source.

27. The memory device, as set forth in claim 26, wherein the first and second transistors are configured to:

receive the disable control signal;

couple the first output terminal and the second output terminal to the low voltage source if the disable control signal corresponds to the deep power down mode; and

isolate the first output terminal and the second output terminal from the low voltage source if the disable control signal does not correspond to the deep power down mode

28. The memory device, as set forth in claim 27, the level shifter comprises a third transistor coupled between the external voltage source and level shifter circuitry, wherein the third transistor is configured to:

receive the disable control signal;

isolate the level shifter circuitry from the external voltage source if the disable control signal does not correspond to the deep power down mode; and

couple the level shifter circuitry to the external voltage source if the disable control signal corresponds to the deep power down mode.

29. A method of achieving low power consumption during a deep power down mode, the method comprising:

receiving an external voltage and a control signal at a regulator control;

grounding a plurality of internal voltage buses at the regulator control if the control signal indicates a deep power down mode; and

providing a plurality of voltages to the plurality of internal voltage buses from the regulator control if the control signal does not indicate the deep power down mode.

30. The method, as set forth in claim 29, comprising the act of isolating the plurality of internal voltage buses from ground if the control signal does not indicate the deep power down mode.

31. The method, as set forth in claim 29, wherein grounding the plurality of internal voltage buses comprises closing a plurality of gates on each of a plurality of transistors to couple the plurality of internal voltage buses to ground.

32. The method, as set forth in claim 29, wherein the plurality of internal voltage buses comprise at least one of an operating voltage bus, a delay lock loop voltage bus, and an array voltage bus.

33. The method, as set forth in claim 29, wherein the plurality of internal voltage buses comprise a booted power voltage bus.

34. A method of providing a deep power down mode, the method comprising:

receiving at least one disable control signal and a data signal at a level shifter;

providing a predetermined output signal when the at least one disable control signal corresponds to a deep power down mode; and

providing an output signal based on the data signal when the at least one disable control signal does not correspond to the deep power down mode.

35. The method, as set forth in claim 34, comprising:

coupling a first output terminal and a second output terminal to ground if the at least one disable control signal indicates the deep power down mode; and

isolating the first output terminal and the second output terminal from ground if the at least one disable control signal does not indicate the deep power down mode

36. The method, as set forth in claim 35, comprising:

isolating the level shifter circuitry from an external voltage source if the at least one disable control signal does not indicate the deep power down mode; and

coupling the level shifter circuitry to the external voltage source if the at least one disable control signal indicates the deep power down mode.

37. The method, as set forth in claim 34, wherein the at least one data signal comprises a first disable signal and a second disable signal.

38. The method, as set forth in claim 37, wherein providing a predetermined output signal comprises coupling an output terminal to an output pad voltage source if the first disable signal indicates the deep power down mode; and

wherein providing an output signal comprises isolating the output terminal from the output pad voltage source if the first disable signal does not indicate the deep power down mode.

39. The method, as set forth in claim 38, wherein providing a predetermined output signal comprises preventing the first transistor from coupling the output terminal to the low output pad voltage source if the second disable signal indicates the deep power down mode; and

wherein providing an output signal comprises permitting the first transistor to couple the output terminal with the output pad voltage source if the second disable signal does not indicate the deep power down mode.

40. The method, as set forth in claim 34, wherein the at least one data signal comprises a first disable signal, a second disable signal, and a third disable signal.

41. The method, as set forth in claim 40, wherein providing a predetermined output signal comprises coupling an output terminal to a low output pad voltage source if the first disable signal indicates the deep power down mode; and

wherein providing an output signal comprises isolating the output terminal from the low output pad voltage source if the first disable signal does not indicate the deep power down mode.

42. The method, as set forth in claim 41, wherein providing a predetermined output signal comprises coupling a gate of a first transistor to an output pad voltage source if the second disable signal indicates to the deep power down mode; and

wherein providing an output signal comprises isolating the gate of the first transistor from the output pad voltage source if the second disable signal does not indicate to the deep power down mode.

43. The method, as set forth in claim 42, wherein providing a predetermined output signal comprises coupling a gate of a second transistor to the low output pad voltage source if the third disable signal indicates to the deep power down mode; and

wherein providing an output signal comprises isolating the gate of the second transistor from the low output pad voltage source if the third disable signal does not indicate to the deep power down mode.